GR-52V002A – Dual N-channel Depletion Mode GaN FET

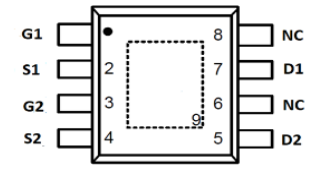
Features

- Typical $R_{DS(ON)}$ = 12Ω (Single Chip)
- Standard Outline For Easy Usage
- Automated Surface Mount Assembly

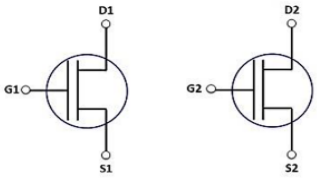
Product Summary

V_{DS}	600	V
$R_{DSon\ max}$	28	Ω
I_{DS}	0.22	A

(TOP VIEW)



SOP-8 (Exposed Pad)



SOP8- Dual Chips
Pin Configuration

Advantages with respect to discrete solutions

- Low BOM count
- Lower assembly cost
- Smaller form factor
- Higher reliability due to less parts and soldering joints

Potential Applications

- AC LED light Engine
- LED filament Bulb
- Smart Lighting & Smart Home

Product Validation

• Qualified for industrial applications according to the relevant tests of JEDEC22

Production Name	Package
GR-52V002A	E-SOP-8

Description

This depletion mode GaN Power Transistor is designed for non-switching applications. This GaN FET has surpassed the JEDEC spec reliability tests of JESD22-A102, JESD22-A104, JESD22-A108, JESD22-A113, JESD22-A118, to just name a few, and therefore provides remark-able manufacturing reliability and reproducibility.

Table of contents

1- Electrical Characteristics and Parameters

➢ Table 1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = -12V)	520	V
V_{GS}	Gate- source voltage	-15 ~ 0	V
I_D	Drain current (continuous) at T_C = 25°C operation (Dual-Chips)	220	mA
	Drain current (continuous) at T_C = 100°C operation (Dual-Chips)	140	mA
$I_{D,pulse}$	Pulsed drain current (V_{DS} = 20V), (Dual-Chips)	400	mA
P_{tot}	Total dissipation at T_C = 25°C Operation	1.20	W

➢ Table 2 Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	(*)Thermal resistance junction-ambient	78	°C/W
T_j	Thermal operating junction-ambient	-55 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

(*) When Mounted on 1 inch^2 FR-4 board, 2 oz of Cu and t = 10 sec.

➢ Table 3 Electrical Characteristics (T_{CASE} = 25 °C)

Static Characteristics

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
$V_{(GS)th}$	Gate threshold voltage	V_{DS}=10V, V_{GS}=-5~0V, I_{DS}=1mA, T_j=25°C	-2.40	-2.20	-2.00	V
$R_{DS(ON)}$	Drain-source on state resistance (Single-Chip)	V_{GS}=0V, I_{DS}=50mA,T_j=25°C	-	12.0	16.0	Ω
$R_{DS(ON),\ Max}$	Drain-source on state resistance (Maximum)	V_{GS}=0V, I_{DS}=50mA,T_j=150°C	-	28.0	-	Ω
B_{VDSS}	Maximum drain-source voltage	V_{GS}=-12V, I_{DS}=100uA	520	-	-	V
I_{DSS}	Drain-source leakage current	V_{GS}=-12V, V_{DS}=650V, T_J=25°C	-	0.05	1.0	uA
I_{GSS}	Gate-source reverse leakage current	V_{DS}=0, V_{GS}= -12V,T_j=25°C	-	0.05	1.0	uA

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
Ciss	Input capacitance	V_{DS} =400V, V_{GS} = -10V,f=1MHz Tj=25℃		10		pF
Coss	Output capacitance			7		pF
Crss	Reverse transfer capacitance			3		pF

2- Typical Characteristic Curves

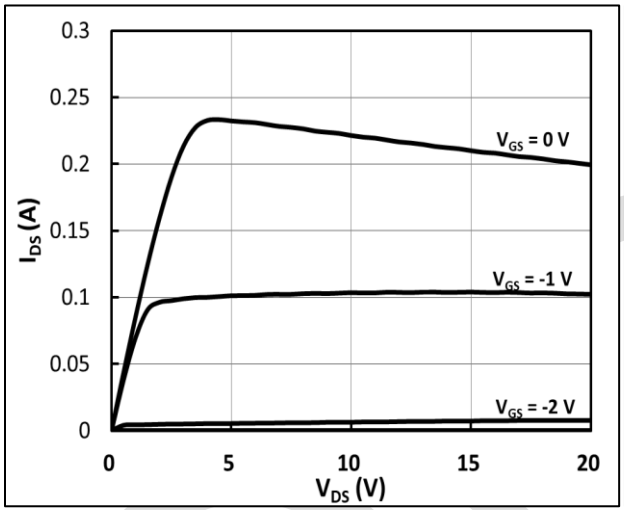


Figure 1: Typical I_{DS} vs. V_{DS} @ T_j=25°C
Parameter: V_{GS}

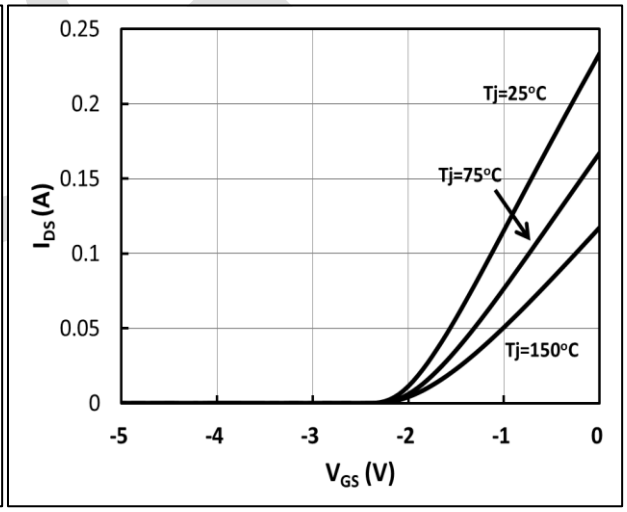


Figure 2: Typical Transfer Characteristics
V_{DS}=10V, Parameter : T_j

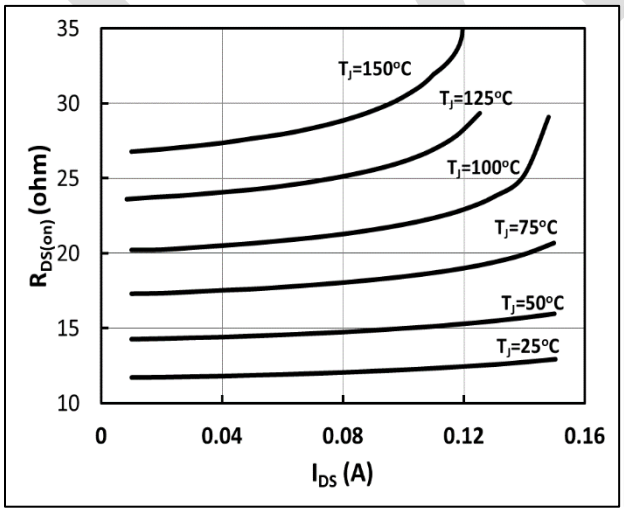


Figure 3: $R_{DS(on)}$ vs. I_{DS} @ V_{GS} = 0V,Parameter: T_j

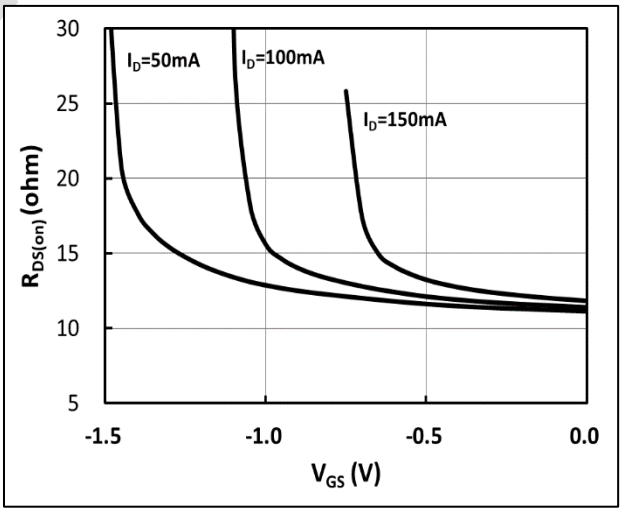


Figure 4: $R_{DS(on)}$ vs. V_{GS} @ T_j = 25°C,Parameter: I_D

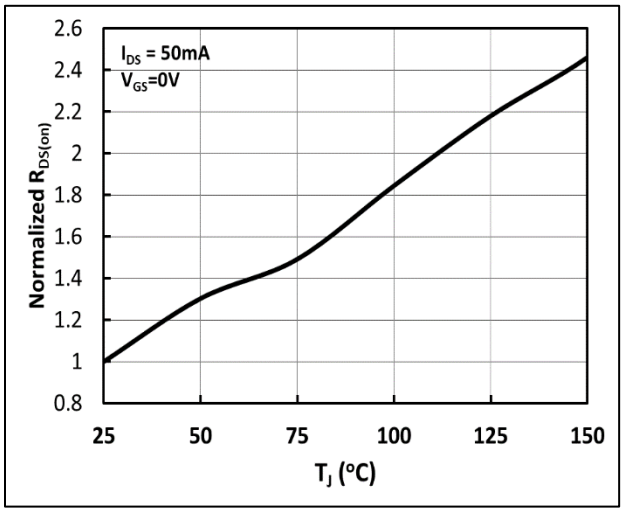


Figure 5: Normalized $R_{DS(on)}$ as a function of T_j

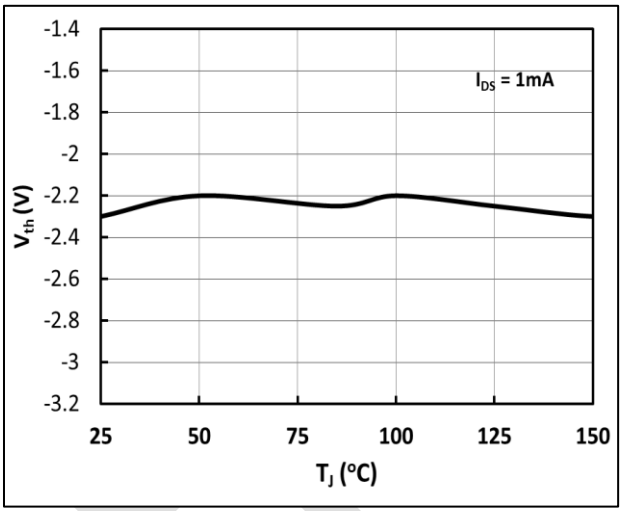


Figure 6: Typical V_{th} vs. T_j @ I_{DS}=1mA

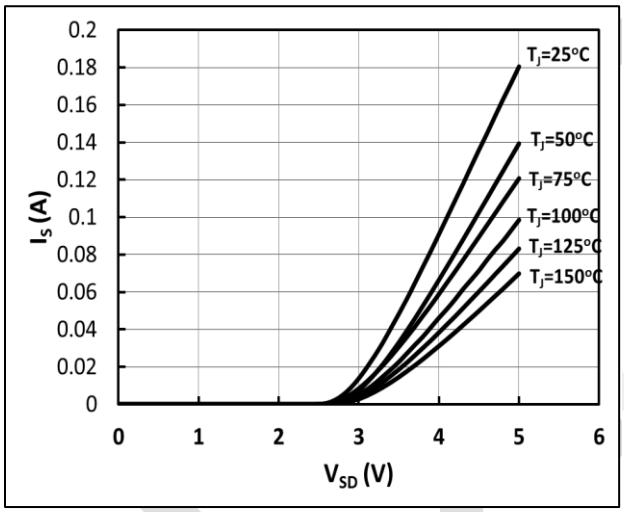


Figure 7: I_S vs. V_{SD} @ V_{GS} = -5V, Parameter: T_j

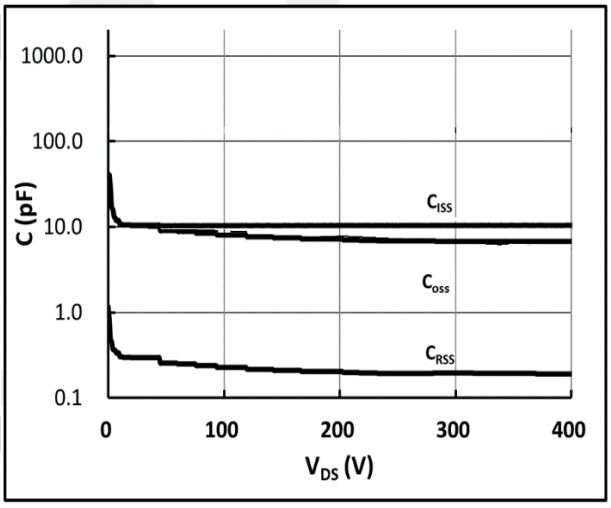
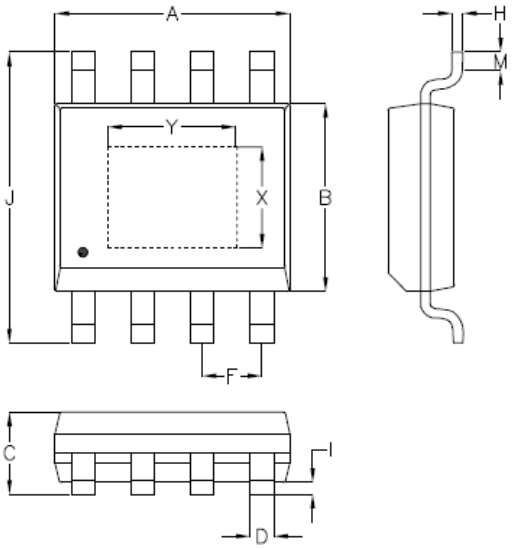


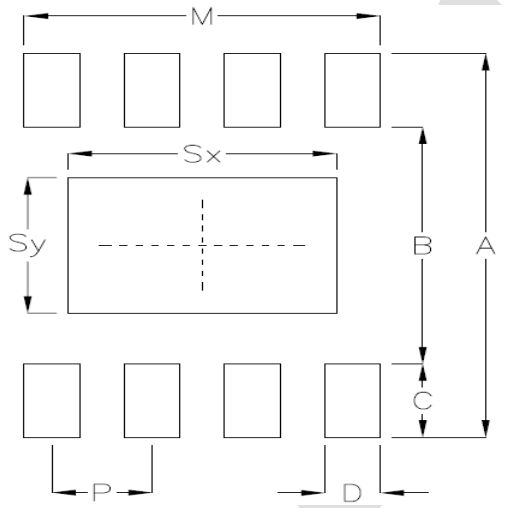
Figure 8 C vs V_{DS}, Parameter: V_{DS}

3- Package dimensions



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option1	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

Figure 9 Package Outline of GR-52V002A Table 4 Dimension of GR-52V002A



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
PSOP-8	8	1.27	6.80	4.20	1.30	0.70	3.40	2.40	4.51	±0.10

Figure 10: Recommended PCB Solder Pad

序号	材料名称	材料规格
01	载带	SOP8: 0.2mm*12mm SOP14/16:0.2mm*16mm
02	盖带	SOP8: 9.3mm SOP14/16:13.3mm
03	纸胶带	10mm WIDE
04	圆盘	13寸
05	圆盘标签	70*50mm
06	内盒标签	70*50mm
07	外箱标签	70*50mm
08	外包装箱	SOP8: 377*350*385mm(60K/箱) SOP14/16:377*285*380mm(40K/箱)
09	保护带	SOP8: 0.2mm*12mm SOP14/16:0.2mm*16mm
10	防静袋/铝箔袋	390*450mm
11	内包装盒	SOP8: 362*362*65mm(12k/盒) SOP14/16:362*362*50mm(8K/盒)
12	黑色保护带	2000*12*0.3mm
13	干燥剂	根据客户要求放入（10.0 g）

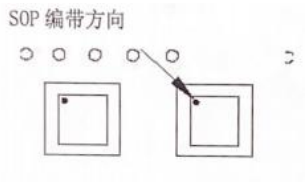


Figure 11 Tape & Reel GR-52V002A

4- Reflow Soldering Profile

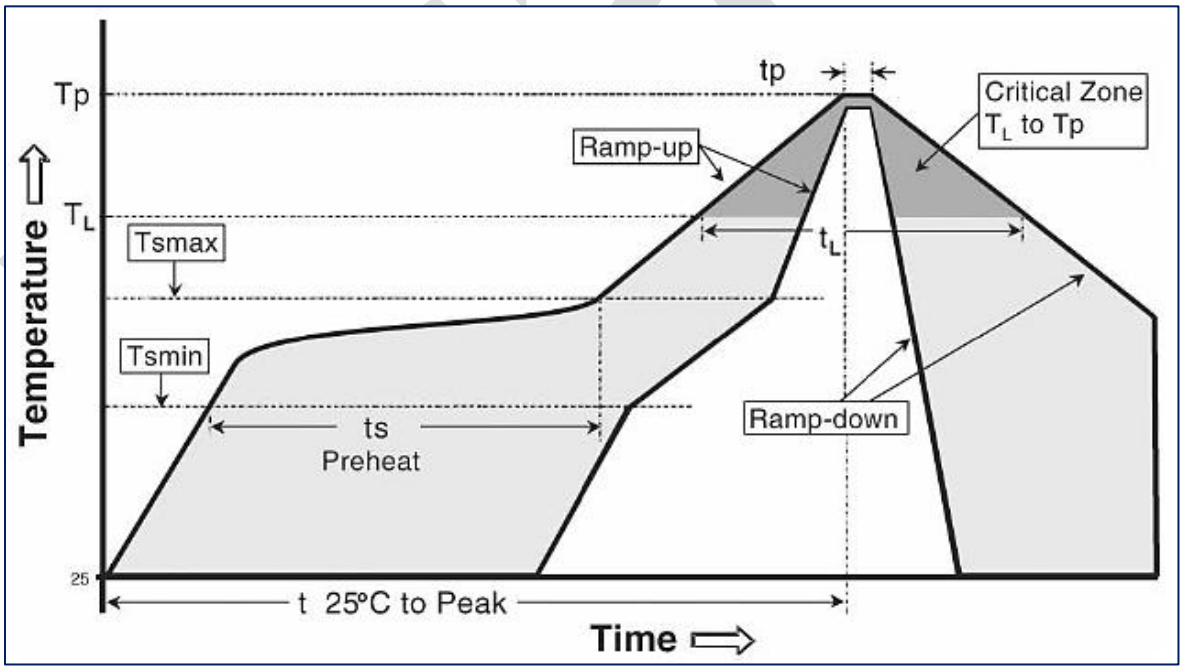


Figure 12 Recommended Reflow Soldering Condition (IPC/JEDEC J-STD-020 Revision C)

Profile Feature		Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)		3 °C/second max.
Preheat	Temperature Min (Tsmin)	150 °C
	Preheat: Temperature Max (Tsmax)	200 °C
	Time (tsmin to tsmax)	60-180 seconds
Time Maintained Above	Temperature (TL)	217 °C
	Time (tL)	60-150 seconds
Peak Temperature (Tp)		260 °C
Time Within 5 °C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6 °C/second max.
Time 25 °C to Peak Temperature		8 minutes max.

Note: All temperatures refer to the topside of the package, measured on the package body surface.

5- Application circuit

One Stage

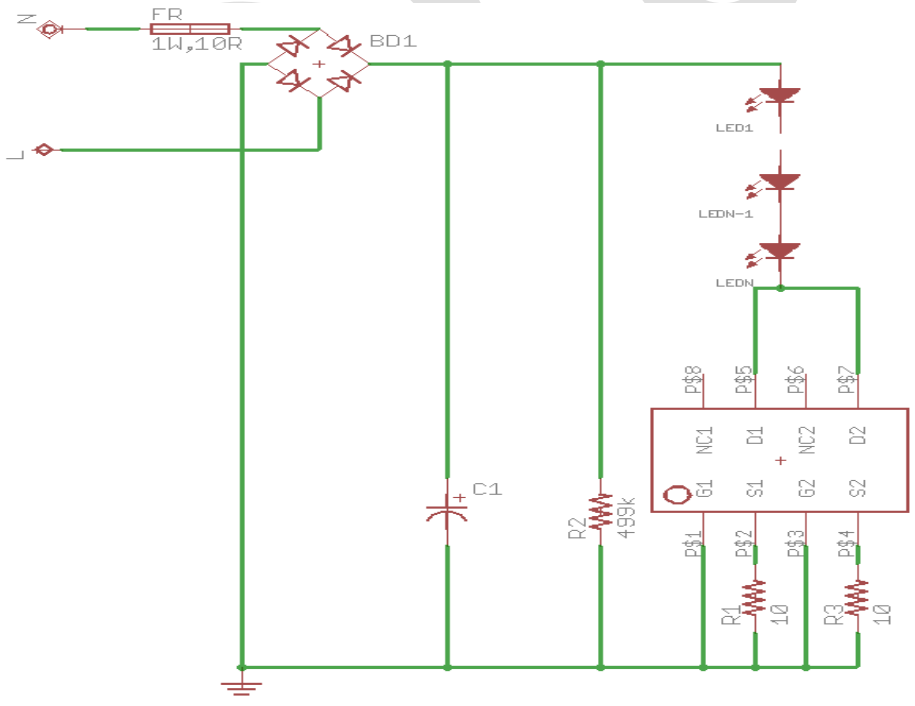


Figure 12 GR-52V002A SOP8 Application non-Dimmable circuit

Item	Qty	Ref Des	Designator	Description	Mfg Part Number	Mfg
1	1	Fuse	F1	10Ω	any	any
2	1	Bridge	BD1	600V, 1A	any	any
3	1	Capacitor	C1	10uF, 400V	Electrolytic capacitor	any
4	1	R1,R3	Resistor	69Ω, 1/8W	SMD:0805	any
5	1	R2	Resistor	499KΩ, 1/4W	SMD:1206	any
6	1	U1	GR-52V002A	520V, 0.2A	SOP-8L	any

Table 6 BOM of Application non-Dimmable circuit

Output current calculate the equation: $\mathbf{Iout} = \frac{-Vth}{Rex+Ron} = \frac{2.2}{Rex+12}\ (A)$

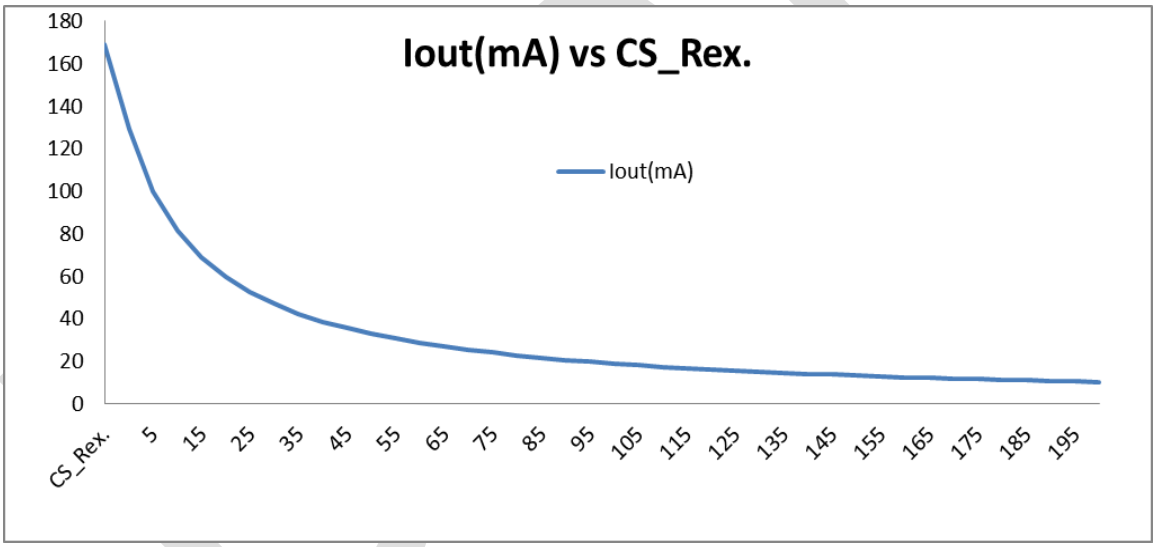


Figure 13 Output Current and CS_resistor curve of SOP-8 (Single Chip)

6- Pin Configuration

Pin No.	Pin Name	Descriptions
1	Gate1	Gate1
2	Source1	Current sense 1,connect the current sense resistor to GND1
3	Gate2	Gate2
4	Source2	Current sense 2,connect the current sense resistor to GND2
5	Drain2	Drain2
6	NC	Not connect
7	Drain1	Drain1 for LED string
8	NC	Not connect
9	Thermal Pad	Not connect

*There are two chips in this SOP-8 Package.

Table 8 Pin Configuration (Dual N-channel GaN FET)

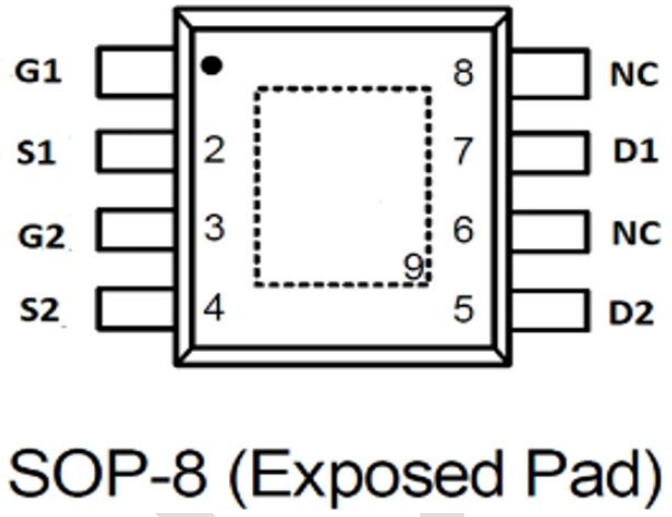


Figure 14 Pin out GR-52V002A

7-Revision History

Date	Revision	Changes
21-Mar.-22	1	First issue