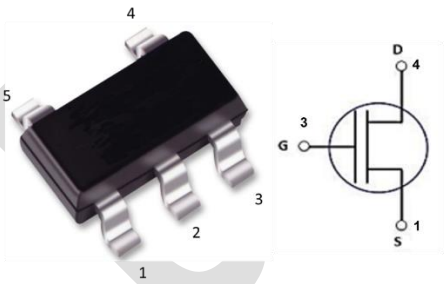
GR-52V001A – N-channel Depletion Mode GaN FET

Features

- Typical $R_{DS(ON)}$ = 14Ω (Single Chip)
- Standard Outline For Easy Usage
- Automated Surface Mount Assembly



SOT-235

Product Summary

V_{DS}	600	V
$R_{DSon\ max.}$	36	Ω
I_{DS}	0.1	A

Advantages with respect to discrete solutions

- Low BOM count
- Lower assembly cost
- Smaller form factor
- Higher reliability due to less parts and soldering joints

Potential Applications

- AC LED light Engine
- LED filament Bulb
- Smart Lighting & Smart Home
- Star up circuit

Product Validation

• Qualified for industrial applications according to the relevant tests of JEDEC22

Production Name	Package
GR-52V001A	SOT-235

Description

This depletion mode GaN Power Transistor is designed for non-switching applications. This GaN FET has surpassed the JEDEC spec reliability tests of JESD22-A102, JESD22-A104, JESD22-A108, JESD22-A113, JESD22-A118, to just name a few, and therefore provides remark-able manufacturing reliability and reproducibility.

Table of contents

1- Electrical Characteristics and Parameters

➢ Table 1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = -12V)	600	V
V_{GS}	Gate- source voltage	-15 ~ 0	V
I_D	Drain current (continuous) at T_C = 25°C operation	100	mA
	Drain current (continuous) at T_C = 100°C operation	50	mA
$I_{D,pulse}$	Pulsed drain current (V_{DS} = 20V),	160	mA
P_{tot}	Total dissipation at T_C = 25°C Operation	0.7	W

➢ Table 2 Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	(*)Thermal resistance junction-ambient	125	°C/W
T_j	Thermal operating junction-ambient	-55 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

(*) When Mounted on 1 inch^2 FR-4 board, 2 oz of Cu and t = 10 sec.

➢ Table 3 Electrical Characteristics (T_{CASE} = 25 °C)

Static Characteristics

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
$V_{(GS)th}$	Gate threshold voltage	V_{DS}=10V, V_{GS}=-5~0V, I_{DS}=1mA, T_j=25°C	-2.50	-2.20	-2.00	V
$R_{DS(ON)}$	Drain-source on state resistance (Single-Chip)	V_{GS}=0V, I_{DS}=50mA,T_j=25°C	-	14.0	20.0	Ω
$R_{DS(ON),\ Max}$	Drain-source on state resistance (Maximum)	V_{GS}=0V, I_{DS}=50mA,T_j=150°C	-	35.0	-	Ω
B_{VDSS}	Maximum drain-source voltage	V_{GS}=-12V, I_{DS}=100uA	520	-	-	V
I_{DSS}	Drain-source leakage current	V_{GS}=-12V, V_{DS}=650V, T_J=25°C	-	0.3	1.0	uA
I_{GSS}	Gate-source reverse leakage current	V_{DS}=0, V_{GS}= -12V,T_j=25°C	-	0.3	1.0	uA

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
Ciss	Input capacitance	V_{DS} =400V, V_{GS} = -10V,f=1MHz Tj=25℃		10		pF
Coss	Output capacitance			7		pF
Crss	Reverse transfer capacitance			3		pF

2- Typical Characteristic Curves

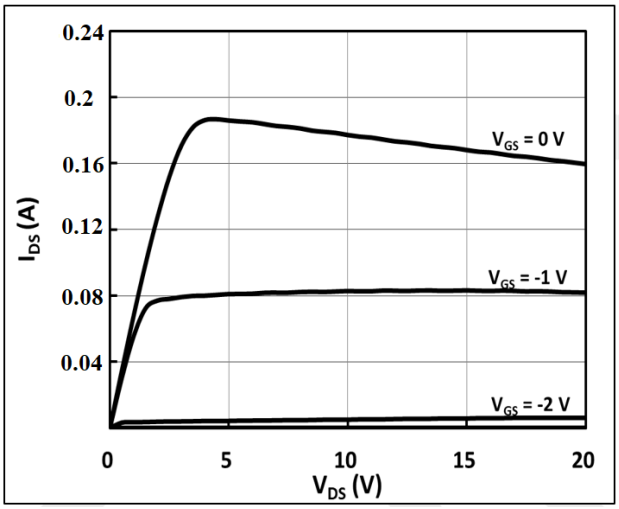


Figure 1: Typical I_{DS} vs. V_{DS} @ T_j=25°C
Parameter: V_{GS}

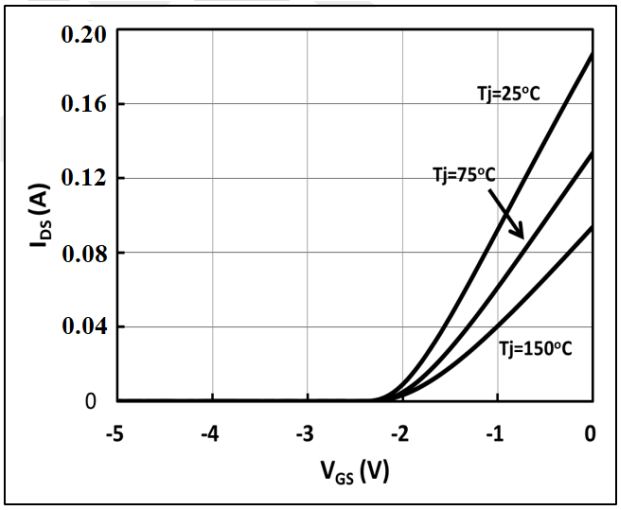


Figure 2: Typical Transfer Characteristics
V_{DS}=10V, Parameter : T_j

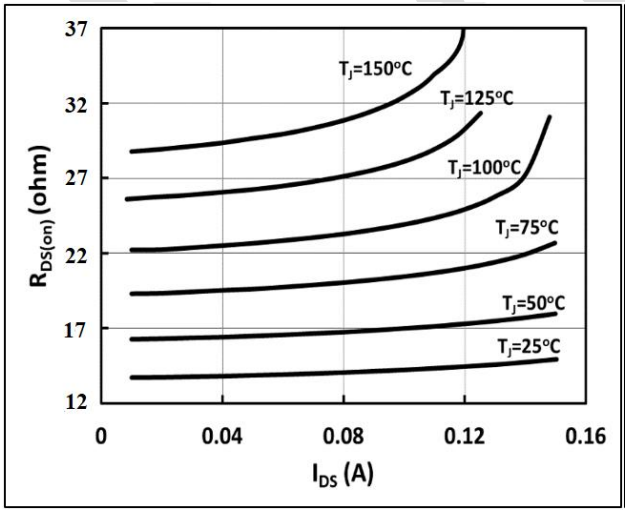


Figure 3: $R_{DS(on)}$ vs. I_{DS} @ V_{GS} = 0V,Parameter: T_j

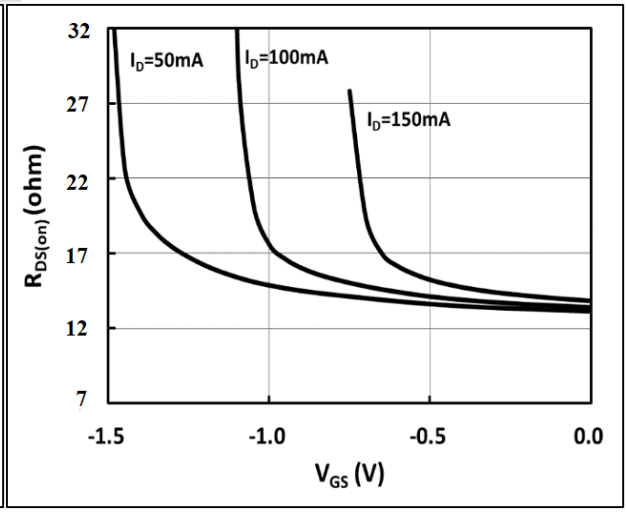


Figure 4: $R_{DS(on)}$ vs. V_{GS} @ T_j = 25°C,Parameter: I_D

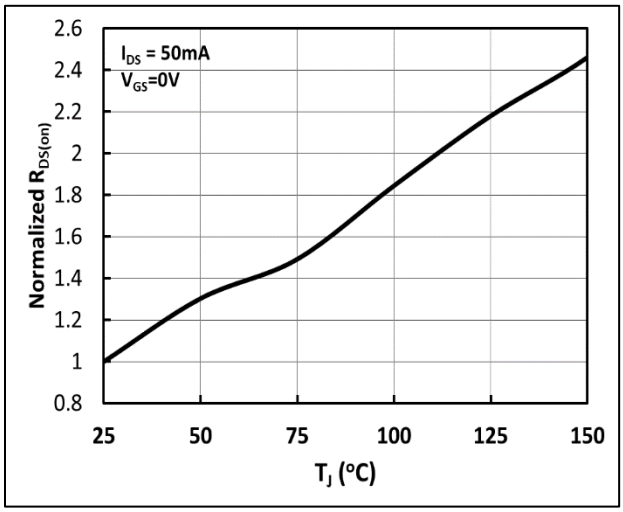


Figure 5: Normalized $R_{DS(on)}$ as a function of T_j

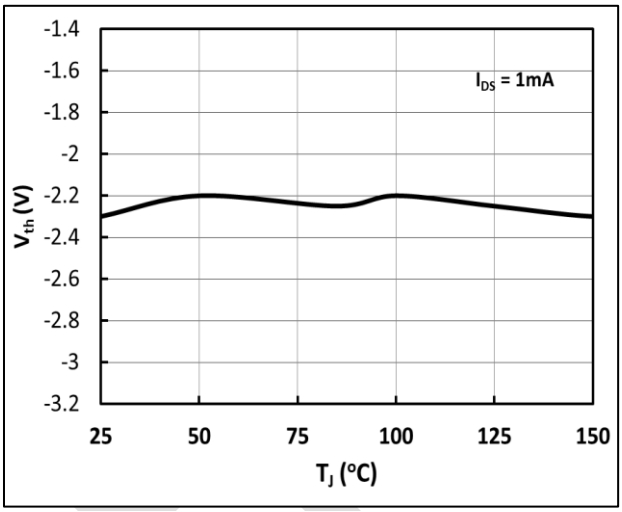


Figure 6: Typical V_{th} vs. T_j @ I_{DS}=1mA

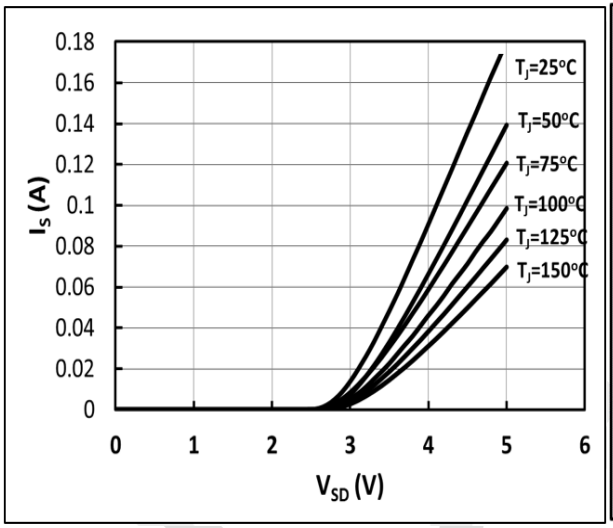


Figure 7: I_S vs. V_{SD} @ V_{GS} = -5V, Parameter: T_j

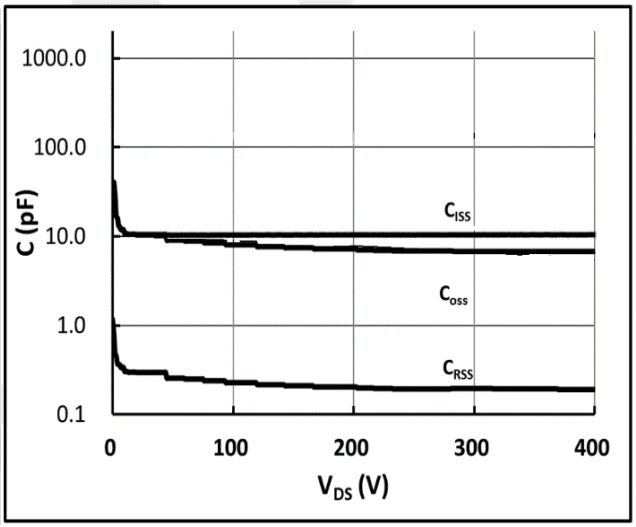
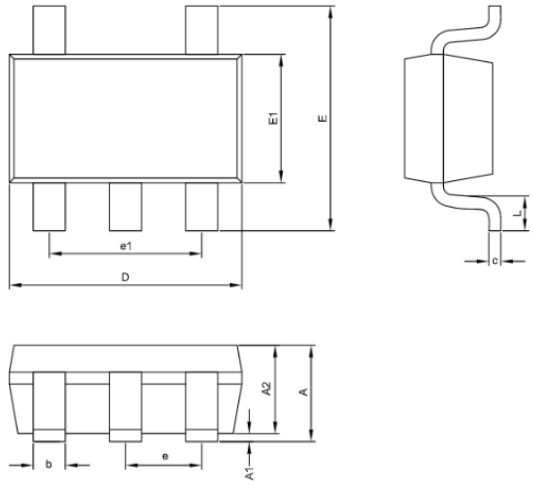


Figure 8 C vs V_{DS}, Parameter: V_{DS}

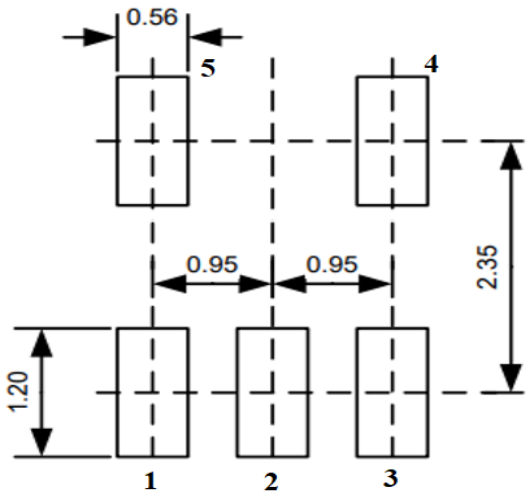
3- Package dimensions



Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.10	1.45	0.039	0.043	0.057
A1	0.00	---	0.10	0.000	---	0.004
A2	1.00	1.10	1.30	0.039	0.043	0.051
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.50	1.60	1.70	0.059	0.063	0.067
c	0.08	0.15	0.25	0.003	0.006	0.010
b	0.30	0.40	0.50	0.012	0.016	0.020
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024

Figure 9 Package Outline of GR-52V001A

Table 4 Dimension of GR-52V001A



* Pin2 is thermal Pin recommended PCB layout Extend copper area min. 6x6 mm^2

Figure 10: Recommended PCB Solder Pad

SOT23封装包装材料（圆盘）

序号	材料名称	材料规格
01	载带	8mm WIDE 4mm PITCH
02	盖带	8mm WIDE
03	保护带	0.2mm*8mm

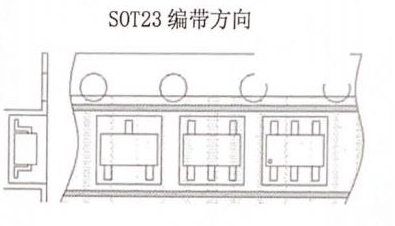


Figure 11 Tape & Reel GR-52V001A

4- Reflow Soldering Profile

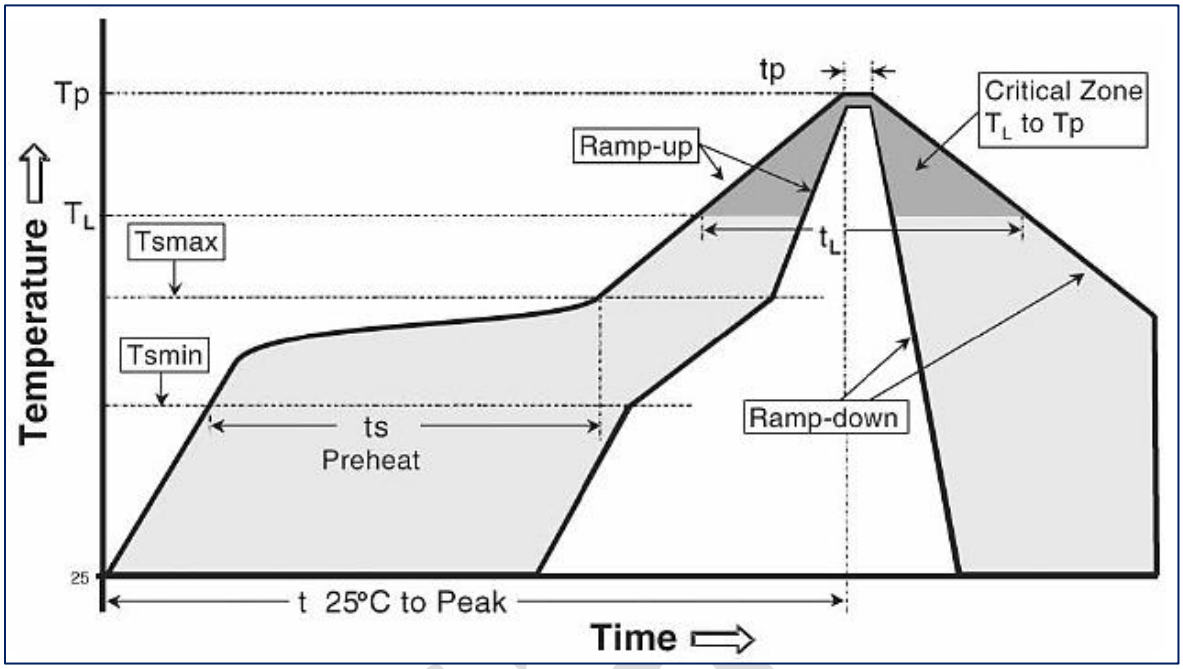


Figure 12 Recommended Reflow Soldering Condition (IPC/JEDEC J-STD-020 Revision C)

Profile Feature		Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)		3 °C/second max.
Preheat	Temperature Min (Tsmin)	150 °C
	Preheat: Temperature Max (Tsmax)	200 °C
	Time (tsmin to tsmax)	60-180 seconds
Time Maintained Above	Temperature (TL)	217 °C
	Time (tL)	60-150 seconds
Peak Temperature (Tp)		260 °C
Time Within 5 °C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6 °C/second max.
Time 25 °C to Peak Temperature		8 minutes max.

Note: All temperatures refer to the topside of the package, measured on the package body surface.

5- Application circuit

One Stage

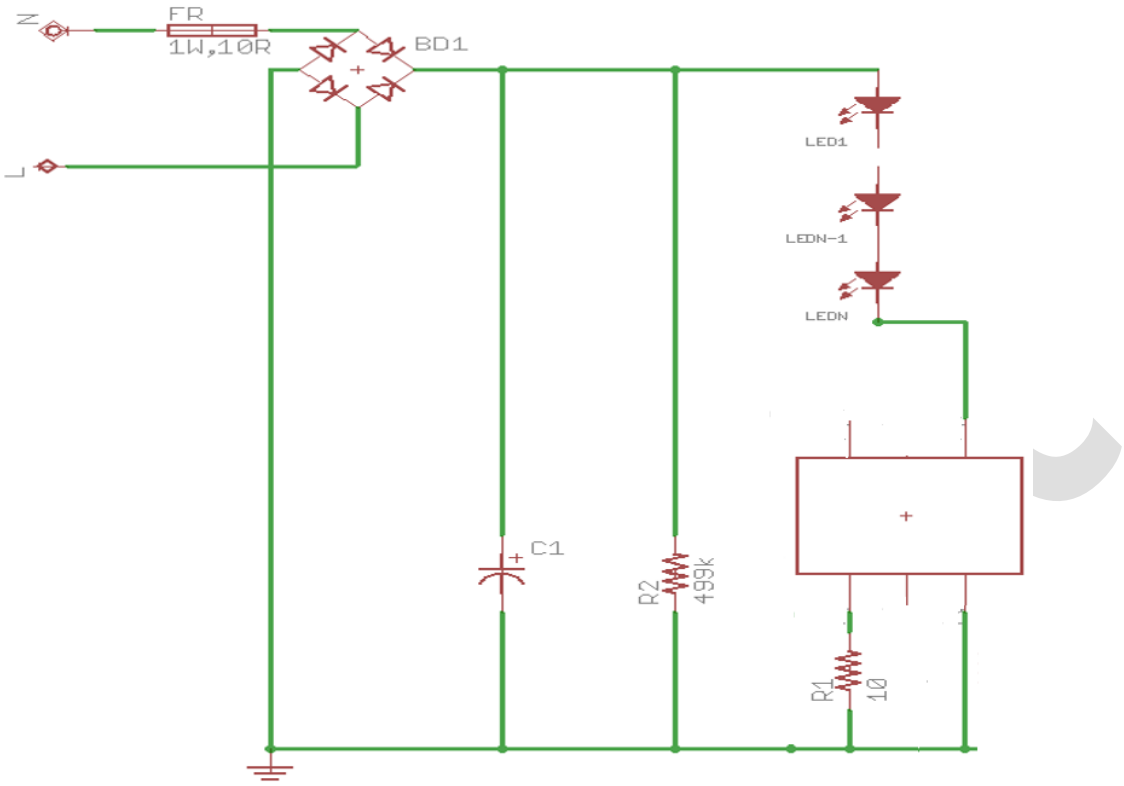


Figure 12 GR-52V001A SOT-235 Application non-Dimmable circuit

Item	Qty	Ref Des	Designator	Description	Mfg Part Number	Mfg
1	1	Fuse	F1	10Ω	any	any
2	1	Bridge	BD1	600V, 1A	any	any
3	1	Capacitor	C1	4.7uF, 400V	Electrolytic capacitor	any
4	1	R1	Resistor	49Ω, 1/8W	SMD:1206	any
5	1	R2	Resistor	499KΩ, 1/4W	SMD:1206	any
6	1	U1	GR-52V001A	600V, 0.1A	SOT-235	

Table 6 BOM of Application non-Dimmable circuit

Output current calculate the equation: $\mathbf{Iout} = \frac{-Vth}{Rex.+Ron} = \frac{2.2}{Rex.+14}\ (A)$

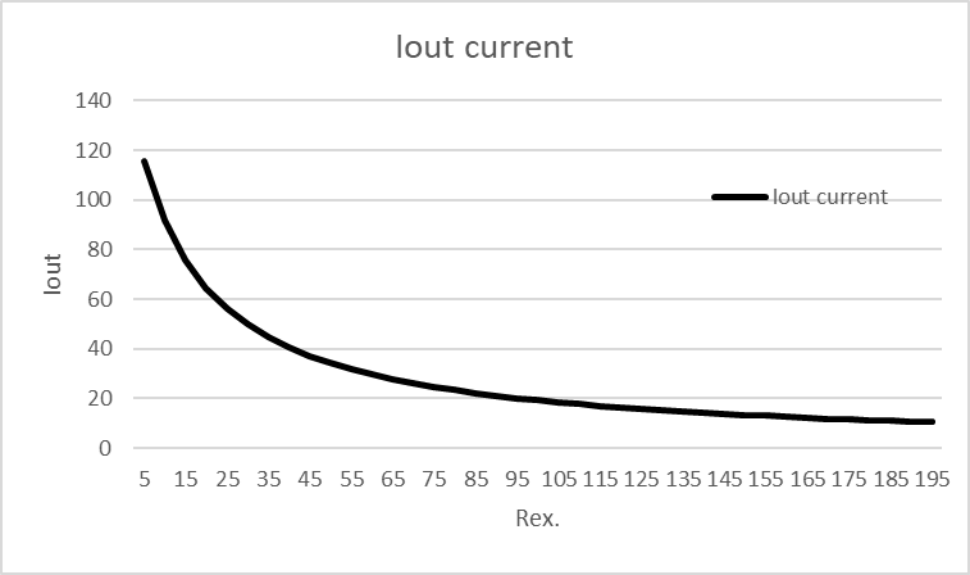


Figure 13 Output Current and Rex. curve of SOT-235 (Single Chip)

6- Pin Configuration

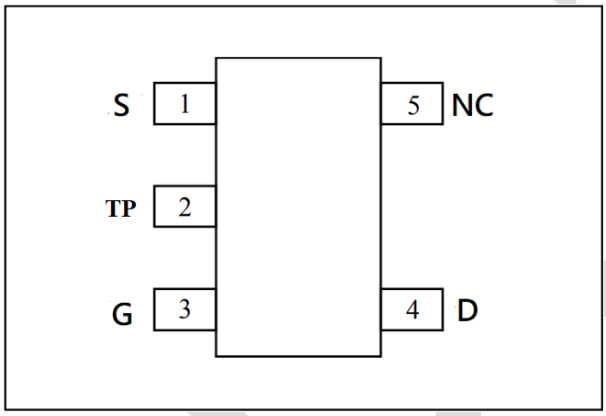


Figure 14 Pin out GR-52V001A

Pin No.	Pin Name	Descriptions
1	S	Current sense, Connect the current sense resistor to Gate
2	TP	Thermal pin-Not connect
3	G	Gate
4	D	Drain
5	NC	Not connect

Table 8 Pin Configuration (N-channel GaN FET)

7-Revision History

Date	Revision	Changes
24-Mar.-22	1	First issue